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VLSI Architecture for Serial Communication Inter–IC Protocol

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Abstract: **The focus of this paper is effectuation of Inter IC (IIC) protocol interface for serial communicating purpose using V H DL and field programmable gate array of Spartan 3E board of cyclone II FPGA. To enable devices to communicate with each other over a serial data bus without data loss. Many serial communication protocols are proposed like SPI, CAN, UART. IIC protocol is advantageous in terms of simplicity of operation, less pin counts etc. Complete operation of Inter IC protocol includes read and write mode of operation. Read and write operation depends on which mode is selected and corresponding signals are generated. The complete module is designed in using active HDL tool of FSM approach and implemented on FPGA using Xiling software.**

Keywords: **IIC, SCL, SDA, VHDL, FPGA.**

I. INTRODUCTION

For various applications embedded system technology is growing rapidly. In embedded system use of microcontroller increases according to that different peripherals are used. Such as, Analog to Digital Converter (A DC), Liquid Crystal Display (LCD), memory and Application Specific IC (ASIC) Serial communication is used to communicate with these peripherals. It is advantageous because, it communicates without shared memory, low pin count and collision rate is low. Different types of serial communication protocols are present like Universal Asynchronous Receiver Transmitter (UART), Control Access Network (CAN), Universal Serial Bus (USB), Serial Peripheral Interface (SPI), Inter-Integrated Circuit (IIC).They are having certain advantage and disadvantage depends on application. SPI and UARTs can communicate from one point to another. USB use multiplexing technique to communicate multiple devices while CAN and I2C use for software addressing of receiver. CAN and SPI protocol are useful.

But design of CAN is complex and have limited portfolio so it is not used in general communication. SPI protocol has advantages of low cost small and easy to design but if peripheral increases the number of interconnects also increases. Hence SPI IS not useful where peripherals are more. I2C is two wire protocol which is easy to design. So, where adjustment of node is to be done and low speed has to be maintained their IIC is useful.

The IIC-bus is used to maximize hardware efficiency and circuit simplicity. All IIC-bus compatible devices have an interface allowing them to communicate directly with each other via the IIC-bus. The concept provides an excellent solution for problems in many interfacing in digital design. IIC is now broadly adopted by many leading chip design companies like Intel, Texas instrument, and Analogy devices *etc*.

II. LITERATURE SURVEY

I2C is one popular serial data transfer protocol and used widely. I2C protocol has many merits such as controllability less wire connection and so on.

In an embedded system physical size of device get reduce. Reduction in size creates a problem of components or IC, interconnects. Philips electronics design protocol for communication between different integrated IC called as Inter IC protocol. Electronics appliances use IIC protocol for communication purpose, I2C bus physically consists of two active wires namely serial clock line (SCL) and serial data line (SDA). SCL and SDA both are active high bidirectional and half duplex in nature [1]. Each device can act as transmitter or receiver depending on its nature. The IIC bus is a of initiating a data transfer on the bus is considered to it. s Low cost and efficient link provide I2C between ICs. It is synchronous

protocol in which master initiate data communication and data get exchanged between master and slave. All communication is control by master using SCL line [1]. All slave connected with SCL line. Slaves are controlled by same SCL line. There are two bidirectional wires SDA and SCL connected to a positive supply voltage via a pull-up resistor [2,4]. The value of pull up register can be given as Consider the VDD related input threshold of VIH = 0.7VDD and VIL = 0.3VDD for the purposes of RC time constant calculation.

$$V(t) = V_{DD}(1 - e^{(\frac{-t}{RC})}$$

Where t is the time since the charging started and RC is the time constant.

If current I flow then resistance can be given as

$$R = \frac{V_{DD} - V_{omax}}{I}$$

Standard value of resistance is $_{Rmax}\,2.95k\sim$

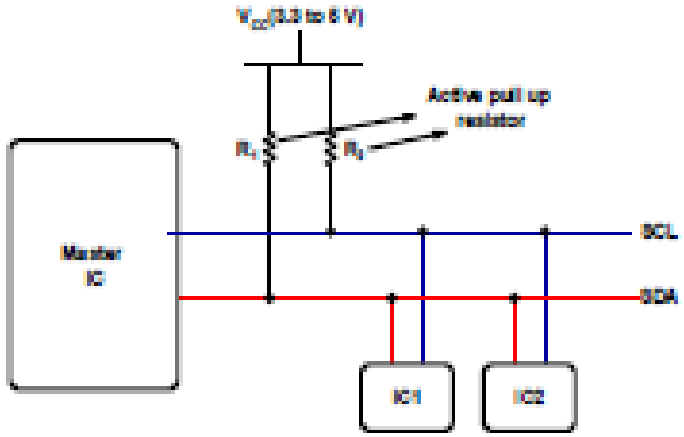


Fig.1 Block Diagram Of Inter IC Protocol

Effective protocol has to design, to increase in speed of operation. Different model proposed by many researchers to implement inter IC protocol which helps to control various applications. Some are summerised below.

For data surveillance purpose Sahu *et al.* developed inter IC protocol. Data surveillance is very important to monitor people/ sensors. Because it could make system efficient, accurate, flexibility, and low development hence IIC is used. . Variable bit rate efficiently uses. With available bandwidth.H.263.Its encoding is very complex. So, normal DSP processor cannot handle it. Hence, FPGA as programmable solution is used. All results were verified using Modelsim.FPGA can be used as interface in between camera and local monitor system [1]

Using system verilog and FPGA, shah *et.al* designed inter IC protocol . This Design mainly includes master and slave design. In medium size FPGA Master design was implemented and its computation was performed on 32 bit Microblaze processor which performs all encryption and decryption.

Some researchers developed Inter-IC protocol with volume controller application. WM 8731 sound driver was used in MP3 audio or speech players. For designed purpose state machine model approach was used because it keeps track of operation from one state to another. A main tool used to design protocol was VHDL and Verilog. Assignment of pins can be done with assignment editor. Joint test action group (JTAG) programming was used and for simulation results validated using Modelsim- Altera 6.5b (Quartos II 9.1) [3].

Jesus lazaro *et al.* A chip to chip communication protocol was proposed using A ES-GCM cryptographic and authentication algorithm. Advanced Encryption Standard (AES) was specification for encryption of electronic data. Galois/Counter Mode (GCM) was mode of operation use to encrypt data because of its efficiency and performance. AES along with GCM algorithm used for secure data flow between devices. Embedded system along with sensor had played vital role in industrial application but problem with system security and privacy of data. Implementation of protocol along with AES-GCM algorithm gives strong computation and flexibility capability along with security of data. [4]

III. DESIGN OF INTER IC PROTOCOL

Main approach to design inter IC protocol is to design in finite state machine approach. For implementing the controller, finite-state machine (FSM) is used. VHDL is popular hardware description languages (HDL) for designing digital circuits. A finite-state machine is a sequential circuit. It uses a finite number of states to keep track of its history of operations. Based on this history and its current inputs, it determines what to do next. I2C protocol design was divided into 3 levels in this method [4], As described in figure 2, these 3 levels from lowest to highest are:

Read and write block, Mid interface level, User interface. For designing inter IC protocol requires different blocks. Main function of protocol is to communicate with slave design. Communication includes read and write operation First step to design read and write block. Design of protocol get divided into different stages

(a) Read and write block

(b) Mid inference

(c) User inference

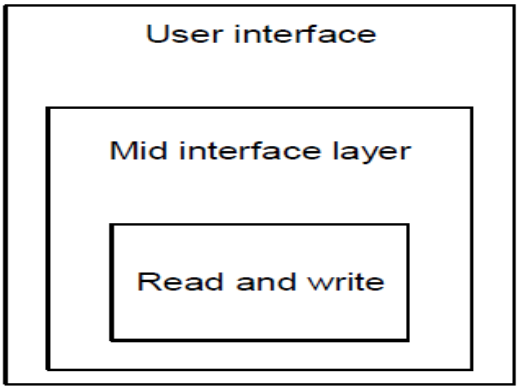


Fig.2 Level Division of IIC Protocol Design

A) Read and Write Block:

Read and write block is lowest level of all three levels. In this level the design was performed according to the protocol control signals and timing. Protocol level is the lowest level of all three levels. Writing and reading are two basic operations in this level. Before reading and writing we have to generate START and STOP signal [1]. Flow diagram for designing read and writes block is as shown in figure.[6]

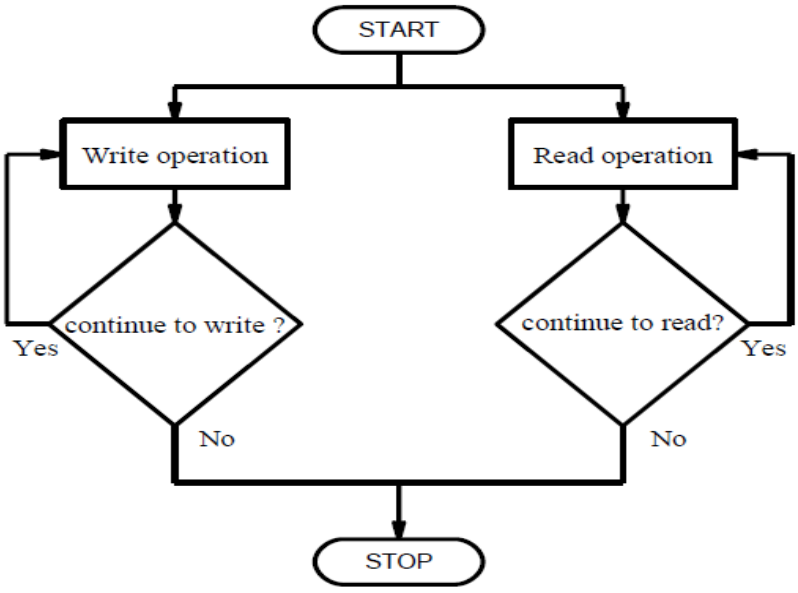


Fig.3 Flow of Read and Write Block

All this design is performed using active HDL tool. Active HDL has tool which is used to design FSM model. Read and write operation is preformed according to frame structure of IIC protocol . Block diagram designed in active HDL is as shown in figure 3. It has different inputs as inSDA, ACKSDA, burstmode, loaddata, start read, startc, stopc, wdata, rs t and clk. And it has diffe rent output as rdata, SCL, SDA, EXDATACLK, ASDA [5]

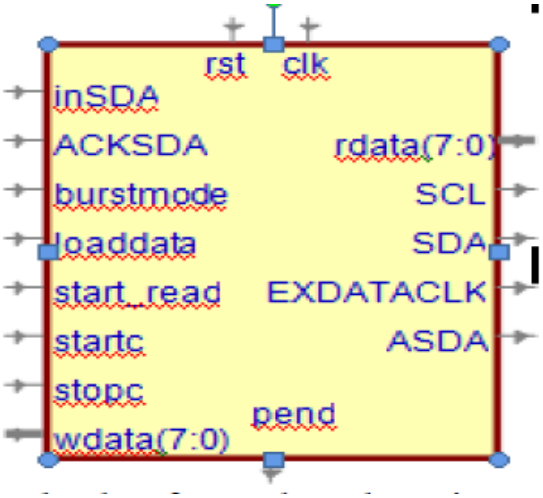


Fig.4 Block of Read and Write Operation

Table 1 Pin description of read and write block

Sr. No.	Pin	Description
1	InSDA	To input data which passes through SDA pin
2	ACKSDA	To Acknowledge the d ata
3	Burstmode	Whether more than 8 bit data has to send
4	Loaddata	If it is '1' then write operation is performed
5	start_read	If it is '1' then read operation is performed
6	Startc	This gives start signal i.e SDA <= '0'; SCL <= '1';
7	Stopc	This gives stop signal i.e SDA <= '1'; SCL <= '1
8	wdata[7:0]	This resistor has 8 bit data which has to write on SDA
9	Clk	This pin has clock in put
10	Rst	If this pin is '1' it reset all functions of block
11	Pend	Pend signal is use to synchronous with midinference
12	SCL	SCL is zoutput serial clock signal
13	SDA	SDA is output serial data signal
14	EXDATACLK	If this signal is '1' then more than 8 bit data is used
15	A SDA	If it is '1' then transmission of 8 bit successfully
16	rdata(7:0)	It store data which get read through in SDA pin

B) M id interference:

Mid interface is used in between user interface and read and write block. Mid interface is used to give signal to read and write block. Also it receive signal from user interface. It receive signal as mode which is of two types as read and write. It also receives address and data of slave.

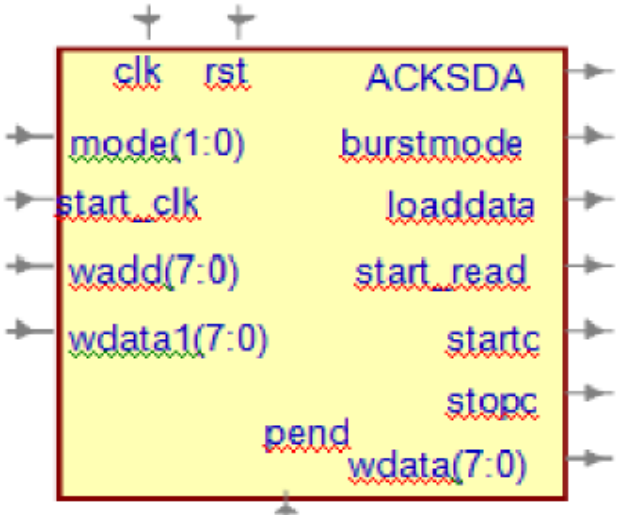


Fig.5 Block diagram mid interface

Table 2: Pin description of mid interface block

Sr. No.	Pin	Description
1	Mode	This pin gives two modes as '01'- write, '10'- read
2	Start_clk	Start clk is input which starts operation of mid inference
3	Wadd (7:1)	Wadd signal gives slave address which is 8 bit address
4	Wdata	Wdata signal gives 8 bit data to slave

C) User interference:

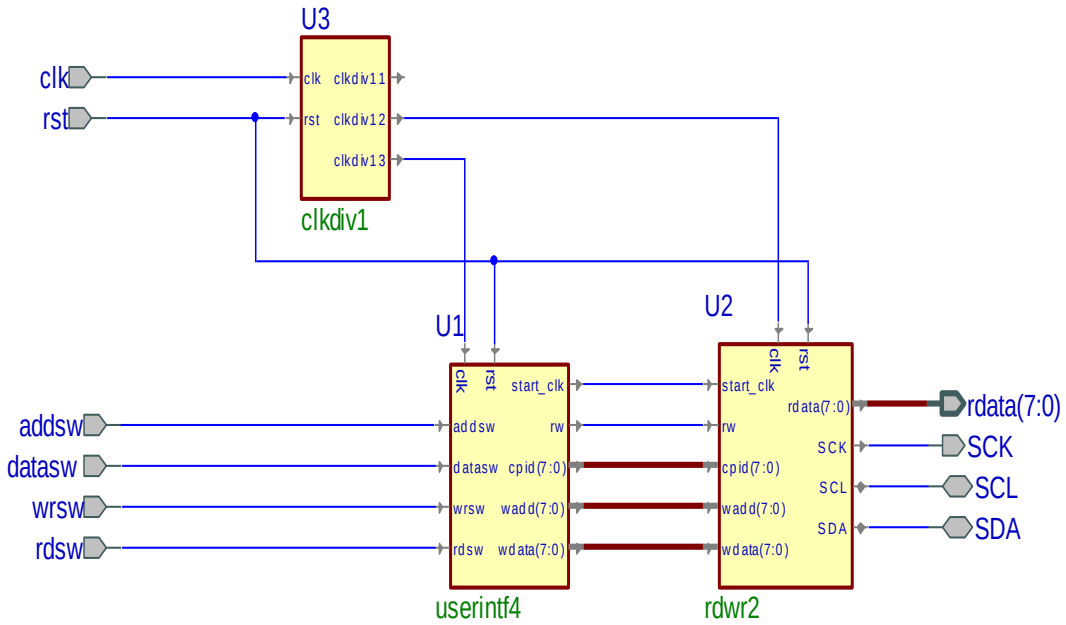
Interface level is the highest level of all three levels. Design of this level was determined by special device. One device can be work in different mode according to system requirement. User interface is designed for interface with FPGA. Hardware has switches as addsw, datasw, rdsw, wrsw. User interference has different signals which can use externally for hardware con necti on.

Fig.6 Block Diagram of User interface

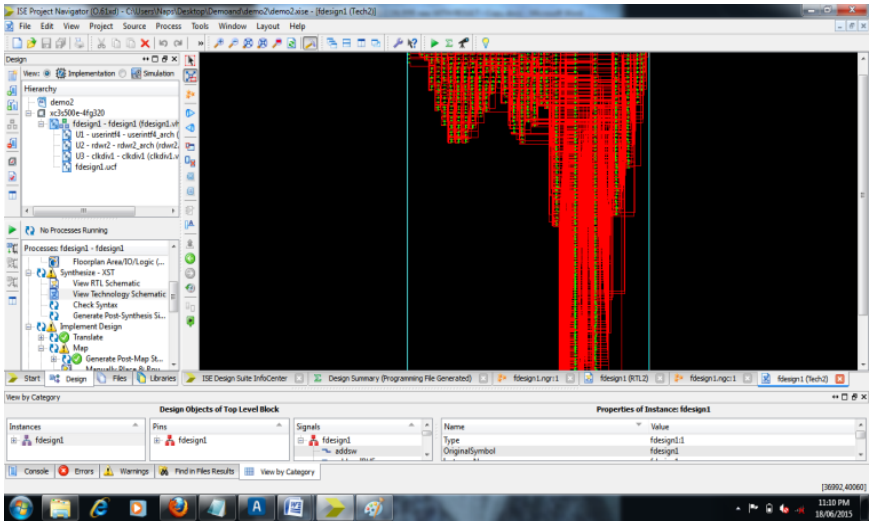
Table 3: Pin description of user interface

Sr. No.	Pin	Description
1	Addsw	Address switch is used to give address of slave to master
2	Datasw	Data switch is used to give data of slave to master
3	Rdsw	Read switch is used to tell that read operation is to performed
4	Wrsw	Write switch is used to tell that write operation is to performed

When all blocks are connected then following setup is form .total four switches to input first is address switch, data switch, read switch and write switch. First input given to address switch which decided the address of slave device after that data switch get which gives particular data to it. Finally, which operation we have performed is decided by read and write switch. Read operation gets data through inSDA pin while write switch writes into register.



Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	267	9,312	2%	
Number of 4 input LUTs	278	9,312	2%	
Number of occupied Slices	258	4,656	5%	
Number of Slices containing only related logic	258	258	100%	
Number of Slices containing unrelated logic	0	258	0%	
Total Number of 4 input LUTs	329	9,312	3%	
Number used as logic	278			
Number used as a route-thru	51			
Number of bonded IOBs	17	232	7%	
Number of BUFGMUXs	3	24	12%	
Average Fanout of Non-Clock Nets	3.19			



IV. RESULT

The propose IIC consist of three blocks read and write block, mid interface, user interface are blocked present in design of IIC Protocol. The propose implementation has a serial communication interface which makes design easy to use and consume less area. The IIC processor describe using the hardware description language VHDL

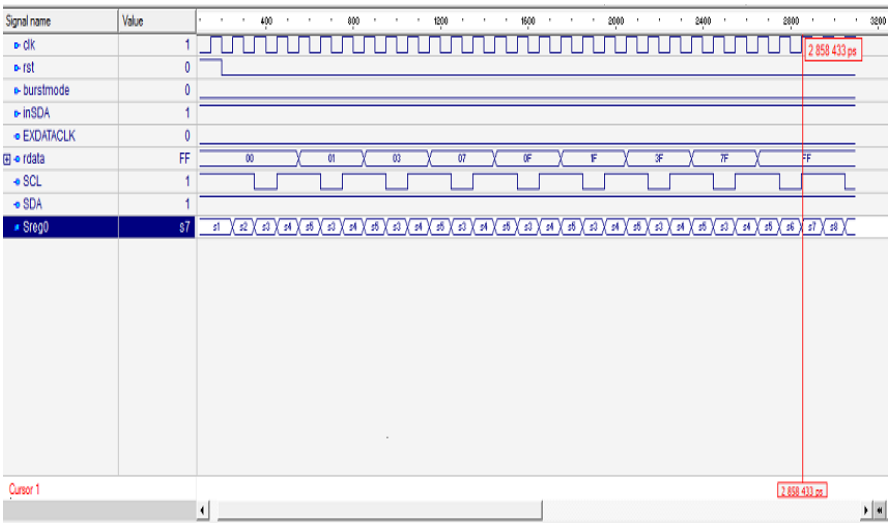


Fig.7 Read Mode Waveform

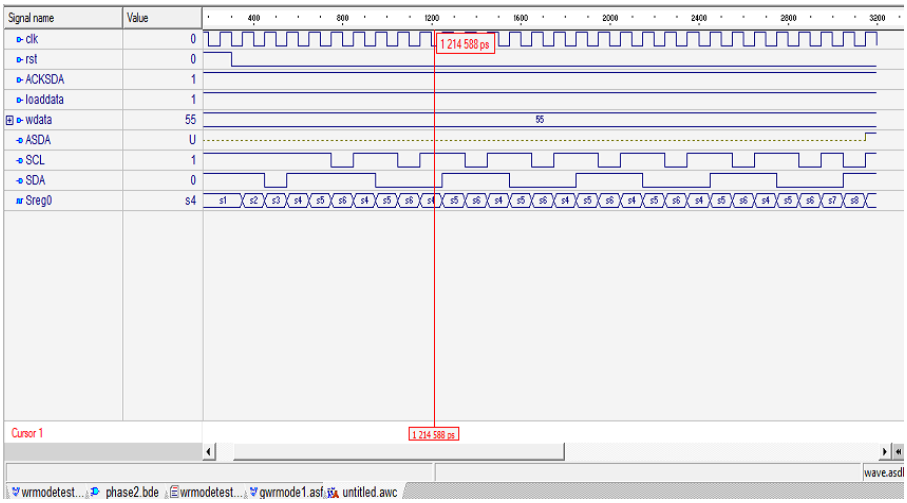


Fig.8 Write Mode Waveform

V. CONCLUSION

In this, IIC protocol having the capability of performance specified, analyzed and implemented using the hardware description language VHDL. The usage of the IIC is flexible, since it has a serial Communication interface that makes the communication with the external world possible. The proposed design is verified on software by timing simulations and on hardware by implementing the design on an FPGA. The design of IIC master controller has immense applications in future as the number of devices connected to a system is only going to increase. So there is always a need for a system which supports multiple protocols. In all these situations, IIC master controller acts as a great support and will be a key in future design to support multiple parallel functions.

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